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Reduced On_Chip Codeword Generation For Cross Talk Effect In Data Transmission Bus

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Abstract:
Today we are having tremendous growth on cross technologies but these technology is limited on interconnected networks. We are having delay for these networks our major goal is prune delay this type of networks but it is dependent on data transmission patterns. Existing bus encoding techniques tackle the issue by avoiding certain types of transitions. These are lack performance and capabilities. Previously proposed many systems these are despite systematic data words on code words. We verify the categorization of the FPF-CAC and show that theoretically but not and practically, a mapping scheme exists between the data words and code words. Our proposed CODEC practical and logical representative design offers a near optimal area overhead performance. An improved version of the CODEC is then presented, which achieves practical optimal performance. This work proposes a code word generation method for such techniques are giving delivers improved rate and reach performance, advanced diagnostics capabilities, standby modes, and more to broadband designers. The system gives effective experimental results.

Key words: CODEC, crosstalk, pruning, shielding.

I.Introduction:

The advancement of very large scale integration (VLSI) technologies has been following Moore's law for the past several decades: In designing a cellular layout, the communications engineer must take account of these various propagation effects, the desired maximum transmit power level at the base station and the mobile units, the typical height of the mobile unit antenna, and the available height of the BS antenna. These factors will determine the size of the individual cell. Unfortunately, as just described, the propagation effects are dynamic and difficult to predict. The best that can be done is to come up with a model based on empirical data and to apply that model to a given environment to develop guidelines for cell size. Operates over new high-performance system-level interconnect technology "Multi-Bit Differential Signaling (MBDS)"Uses inherent properties of MBDS to achieve error control while requiring minimal data and logic overhead. Future global wires will function as lossy transmission lines Reduced-swing signaling Noise due to crosstalk, electromagnetic interference, and other factors will have increased impact.it will not be possible to abstract the physical layer of on-chip networks as a fully reliable, fixed-delay channel At the micro network stack layers atop the physical layer, noise is a source of local transient malfunctions. Non-scalable global wire delay Moving signals across a large die within one clock cycle is not possible.Current interconnection architecture- Buses are inherently non-scalable. Transmission of digital signals along wires is not reliable.

II. Related Work

As the crosstalk is dependent on the data transition patterns on the bus, patterns can be classified based on the severity of the crosstalk they impose on the bus The theoretical lower bound of the area overhead for memory-based codes is lower compared to memory-less codes. However, the memory-based CODECs are much more complex and the only known code word generation method is an exhaustive search and pruning based method As stated in the previous section, the degree of crosstalk in an on-chip bus is dependent on data transition patterns on the bus. In the meanwhile, however, DSM technologies also present new challenges to designers on many different fronts such as (i) scale and complexity of design, verification and test; (ii) circuit modeling and (iii) processing and manufacturability. Innovative approaches are needed at both the system level and the chip level to address these challenges and mitigate the negative effects they bring. Several methods have been proposed to eliminate/reduce Cross talk delay. Some of these methods are based on routing strategies [5, 6,7, 8], which employ various routing techniques to minimize

crosstalk delay within a data-path or logic block. Repeater insertion techniques are used to reduce capacitance and resistance of long interconnections for decreasing wire delay [2, 4]. But these techniques cannot solve the problem of simultaneous transitions for opposite directions. In order to overcome this problem, a bus delay reduction technique was proposed in [8]. The main idea is to prevent simultaneous opposite transitions by skewing signal transition timing of adjacent wires.

III Proposed System:

This paper focuses on the overcome of the limitations of FPF-CAC. The lack of practical CODEC construction schemes has hampered the use of such codes in practical designs. This work presents guidelines for the CODEC design of the forbidden pattern free crosstalk avoidance ode‖(FPF-CAC). We analyze the properties of the FPF-CAC and show that mathematically, a mapping scheme exists. In this paper, we offer a systematic CODEC construction solution for the forbidden-pattern-free crosstalk avoidance code (FPF-CAC). The mapping scheme we propose is based on the recursive procedure . We propose several different coding schemes that allow the CODECs to be constructed for any arbitrary bus size. With such a systematic mapping, the CODEC for a wider bus is constructed by a simple extension of the CODEC for a smaller bus. The first CODEC proposed in the paper is proven to have near-optimal area overhead performance. We further offer an improved coding scheme that achieves optimal overhead performance. We also propose modifications to our near-optimal CODEC that will reduce the complexity and improve the delay performance of the CODEC. The key contributions of this paper include the following.

1) We define a deterministic mapping scheme for the FPF-CAC.
2) Based on the mapping scheme, we propose coding algorithms that allow systematic CODEC constructions so that the CODEC for a wider bus is obtained as an extension of the CODEC for smaller bus.
3) We show that the CODEC gate count grows quadratically with bus size as opposed to the exponential growth for the existing approaches.
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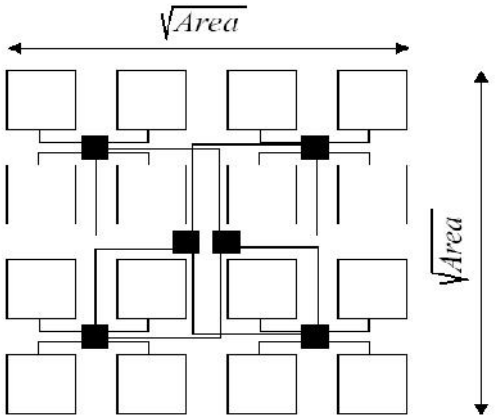

Fig 1:communication pipeline

IV Conclusion:

FNS-based FTF encoding algorithms are very efficient in terms of area overhead. In this work, we presented a novel method to avoid crosstalk using Forbidden Transition Free, Fibonacci Number System CODEC. This work is much superior in terms of Speed, Power consumption and Area required for implementing this CODEC. This CODEC has got an improved speed of around 2.5 times than the implementation technique. In this paper, we give what we believe is the first solution to this problem. We showed that data can be coded to a forbidden pattern free vector in the Fibonacci numeral system. We first give a straightforward mapping algorithm that produces a set of FPF codes with near-optimal cardinality. The area overhead of this coding scheme is near the theoretical lower bound. The CODEC based on this coding scheme is systematic and has very low complexity. The size of the CODEC grows quadratically with the data bus size as opposed to exponentially in a brute forced implementation. Our systemic coding scheme allows the code design of arbitrarily large busses without having to resort to bus partitioning.

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